23. (New) The method of claim 21, wherein the wafer comprises a plurality of adjacent die pads and a single scribe lane separates each die pad from the adjacent die pads.

24. (New) The method of claim 23, wherein the scribe lane comprises a single row of gettering plugs, a pair of parallel rows of gettering plugs or a pair of parallel gettering trenches.

25. (New) The method of claim 21, wherein the dopant is one or more selected from phosphorus, arsenic, antimony, bismuth, boron, aluminum, gallium, indium, helium, neon, argon, krypton, xenon and germanium.

REMARKS

Upon entry of the present Reply, claims 1-15 and 21-25 are pending in the application. Claims 16-20 are canceled herein. Claims 2, 3, 10 and 12-14 have been amended herein. These claims are amended to correct the dependency of claims 12-14 and to clarify the antecedent basis for the terms used in claims 2, 3 and 10. These amendments are not narrowing amendments, and do not surrender any subject matter. No new matter is contained in these amendments.

New claims 21-25 have been added herein. New claims 21-25 are supported in the claims as originally filed and in the specification as originally filed. Support for new claim 21 is found, for example, in original claims 9, 12 and 14, and at page 6, lines 6-16. Support for new claim 22 is found, for example, in original claim 15. Support for new claim 23 is found, for example, in Fig. 1. Support for new claim 24 is found, for example, at page 7, lines 5-9. Support for new claim 25 is found, for example, in original claims 3 and 10. No new matter is included in the newly submitted claims.

Claims 1-15 have been rejected in the Office Action to which the present Reply is responsive. Based on the present Reply, Applicant respectfully requests reconsideration and

withdrawal of the rejections of Applicant's claims, and passage of the present application to allowance and issue.

The specification is amended to reflect the drawing corrections submitted herewith.

REJECTIONS OVER HATTORI ET AL AND MASZARA

In the Office Action, claims 1-15 were rejected under 35 U.S.C. § 103(a) as obvious over Hattori et al (U.S. Patent 6,252,294) in view of Maszara (U.S. Patent 6,444,534). The Examiner asserted that Hattori teaches various elements of the claimed invention, but admitted that Hattori fails to teach all the features of the claimed invention. The Examiner cited and relied upon Maszara in order to remedy the admitted deficiencies of Hattori. Applicant respectfully traverses the rejections over Hattori in view of Maszara for the following reason.

Maszara is not citable as prior art against the present application. Maszara is assigned to the same person as the present application, and is prior art against the present application only under 35 U.S.C. § 102(e). As set forth in 35 U.S.C. § 103(c), subject matter developed by another person, which qualifies as prior art only under 35 U.S.C. § 102(e), shall not preclude patentability under 35 U.S.C. § 103 where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.

Application No. 09/824,933 (the present application) and U.S. Patent No. 6,444,534 were, at the time the invention of Application No. 09/824,933 was made, owned by Advanced Micro Devices, Inc., of Sunnyvale, California. This constitutes Applicant's statement of common ownership regarding the cited art, in accordance with MPEP 706.02(I)(2).

Applicant respectfully submits that for at least the reasons admitted by the Examiner, Hattori fails to disclose or suggest Applicant's presently claimed invention. Accordingly, Applicant respectfully requests the Examiner to reconsider and withdraw the rejection of Applicant's claims over the prior art, and to indicate that the claims are allowable. Applicant respectfully requests notice to such effect.

Applicant respectfully submits that the newly submitted claims 21-25 are allowable over the art of record for the same reasons as claims 1-15 are allowable thereover.

REQUEST FOR INITIALED COPY OF INFORMATION DISCLOSURE STATEMENT

On April 23, 2001, Applicants filed an Information Disclosure Statement. An initialed copy of the April 23, 2001 IDS was not included with the present Office Action. Accordingly, Applicant respectfully requests the Examiner to provide an initialed copy of the PTO-1449 included with the April 23, 2001 IDS, indicating that the references cited therein have been considered by the Examiner. For the convenience of the Examiner, a copy of the IDS, PTO-1449 and Applicant's Transmittal Form, showing that these papers were in fact filed on April 23, 2001, are included with this Reply to Office Action. Appropriate indication of the Examiner's consideration of the references cited in the April 23, 2001 IDS is requested.

Applicant notes that initialed copies of the forms PTO-1449 submitted with the IDSs filed February 4, 2002 and March 27, 2002 were included in the Office Action.

FORMAL DRAWINGS

Applicant submits herewith a corrected drawing sheet, with the requested changes marked in red ink. Applicant files together with this Reply a Submission of Corrected Formal Drawing, including a revised drawing sheet including the changes to Fig. 1 indicated in the above-noted corrected drawing sheet. Appropriate consideration and entry of this corrected drawing sheet is respectfully requested. In addition, Applicant submits herewith a correction of the specification, in which reference to the line "A-A" is corrected to refer to line "2-2" in accordance with the change to Fig. 1 submitted herewith. Appropriate correction of the specification is requested.

CONCLUSION

For the foregoing reasons, Applicant respectfully requests the Examiner to reconsider and withdraw the rejections of Applicant's claims, and to allow the presently pending claims. Notice of Allowance is respectfully requested.

In the event issues remain in the prosecution of this application, Applicants request that the Examiner telephone the undersigned attorney to expedite allowance of the application. Should a Petition for Extension of Time be necessary for the present Reply to the outstanding Office action to be timely filed (or if such a petition has been made and an additional extension is necessary) petition therefor is hereby made and, if any additional fees are required for the filing of this paper, the Commissioner is authorized to charge those fees to Deposit Account #18-0988, Docket No. F0556.

Respectfully submitted,
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DATE: September 27, 2002

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APPENDIX

The paragraphs at page 4, lines 2-7, as shown above, have been amended as follows:

Fig. 2 is a schematic cross-sectional view, taken along line **[A-A]** 2-2 of Fig. 1, of a first embodiment of a scribe lane gettering plug on an SOI wafer, in accordance with the present invention.

Fig. 3 is a schematic cross-sectional view, taken along line **[A-A]** 2-2 of Fig. 1, of a second embodiment of a scribe lane gettering plug on an SOI wafer, in accordance with the present invention.

The paragraphs at page 6, lines 6-25, as shown above, have been amended as follows:

Fig. 2 shows a partial cross-sectional view of a portion of a gettering plug 108 taken along line **[A-A]** 2-2 in Fig. 1. Fig. 2 shows a portion of the SOI wafer 100, including the silicon active layer 102, a buried oxide layer 110 and a silicon substrate 112. Fig. 2 indicates by vertical dashed lines an approximate area of a scribe lane 106. It will be recognized that the width of the scribe lane 106 may extend to the edge of the die pad 104. The SOI wafer 100 shown in Fig. 2 further includes a gettering plug 108. The gettering plug 108 may be separated from the silicon active layer 102, and thereby from the die pads 104 and the semiconductor devices thereon, by a sidewall liner 114. In Fig. 2, the gettering plug 108 extends through both the silicon active layer 102 and through the dielectric insulation layer 110 of the SOI wafer 100. In one embodiment, the SOI wafer 100 does not include a sidewall liner.

Fig. 3 shows a partial cross-sectional view of a portion of a second embodiment of the gettering plug 108, taken along line **[A-A]** 2-2 in Fig. 1. Like Fig. 2, Fig. 3 shows a portion of the SOI wafer 100, including the silicon active layer 102, the buried oxide layer 110 and the silicon substrate 112. Fig. 3 indicates by vertical dashed lines the approximate area of the scribe lane 106, and includes the gettering plug 108. The gettering plug 108 is separated from the silicon active layer 102, and thereby from the die pads 104 and the semiconductor devices thereon, by a sidewall liner 114. In Fig. 3, the gettering plug 108 extends through the silicon active layer 102, down to but not through the dielectric insulation layer 110 of the SOI wafer 100.

The amended claims shown above have been amended as follows:

2. (Amended) The method of claim 1, wherein the doped fill material is polysilicon formed by LPCVD deposition of the polysilicon and **[the]** **a** dopant in the cavity.

3. (Amended) The method of **[claim 1]** **claim 2**, wherein the dopant **[ions are]** **is** one or more selected from phosphorus, arsenic, antimony, bismuth, boron, aluminum, gallium, indium, helium, neon, argon, krypton, xenon and germanium.

10. (Amended) The method of claim 9, wherein the dopant **[ions are]** **is** one or more selected from phosphorus, arsenic, antimony, bismuth, boron, aluminum, gallium, indium, helium, neon, argon, krypton, xenon and germanium.

12. (Amended) The method of **[claim 10]** **claim 9**, wherein the fill material is polysilicon, and the dopant is added by one of codeposition and implantation.

13. (Amended) The method of **[claim 10]** **claim 9**, wherein the gettering plug extends through the silicon active layer, and contacts a dielectric insulation layer on the wafer.

14. (Amended) The method of **[claim 10]** **claim 9**, wherein the gettering plug extends through both the silicon active layer and a dielectric insulation layer on the wafer.